A Merged Structure of LNA & Sub-Harmonic Mixer for Multi-band DCR Applications

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***Abstract* — A merged structure of variable gain LNA and sub-harmonic mixer is designed for multi-band direct conversion receiver (DCR) application with a 0.18μm CMOS process. The circuit uses inductive peaking load to increase 3dB-bandwidth and achieves 22.7~32dB conversion gain, 2.8~4.1dB DSB NF, -10.5~4.1dBm IIP3 and 5~17.3dBm IIP2 from 800MHz to 2.4GHz input range. Variable gain range is 11.5dB at 2.1GHz and typical LO to RF isolation is less than -50dBm and DC offset voltage is less than 10mV. The overall power consumption is 17mW with 1.8V supply voltage and chip size is 2.3mm×1.2mm.**

I. INTRODUCTION

Current trend in RFIC design is a realizing multi-band and multi-mode RF transceiver on a single chip to reduce cost and to accommodate various wireless communication standards [1]. To implement single chip transceiver, direct conversion receiver (DCR) is a very promising solution [2]. However, the DCR system must solve DC offset and 1/f noise problem. In this paper, to realize multi-band DCR system, we propose a merged structure of differential variable gain LNA and sub-harmonic IQ mixer as a RF front-end receiver circuit, which adopts inductively folded cascode structure to increase bandwidth and minimize non-linear and noisy elements.

II. CIRCUIT DESIGNS

Basic concepts of conventional mixer and proposed merged structure of LNA and sub-harmonic mixer (SH-mixer) are shown in Fig.1 (a) and (b) respectively. In each case, if we assume that the LO voltage is an ideal square wave and very large enough to fully turn on and off the switching transistor, then the down-conversion signals are expressed as followings.

$$V_{IF,conventional} = 2K_C V_{RF}\cos w_{RF}t \times \sum_{n=1}^{\infty}\left(\frac{\sin(n\pi/2)}{n\pi/2}\cos nw_{LO}t\right) \quad (1)$$

$$V_{IF,sub-harmonic} = 2K_S V_{RF}\cos w_{RF}t \times \sum_{n=1}^{\infty}\left(2\times\frac{\sin(n\pi/4)}{n\pi/2}\cos n\frac{w_{LO}}{2}t\right) \quad (2)$$

In each expression, $V_{RF}\cos w_{RF}t$ means RF input signal, K_C, K_S are gain factors, usually expressed as the product of trans-conductance of input transistor (G_m) and load resistance (R_L), and we assume that the mixers operate in the double-balanced mode. The role of switching transistor (Q_s) is evenly distributed to two parallel-connected transistors (Q_{s1},Q_{s2}) in SH-mixer, thus it needs only half LO frequency compared to conventional mixer, which eliminates DC offset problem originated from self-mixing of large LO signal. Another important feature in the proposed structure is that LNA replaces G_m-cell of the conventional mixer to minimize non-linear and noisy elements. More specific circuits of the proposed structure are shown in Fig. 2 (a).

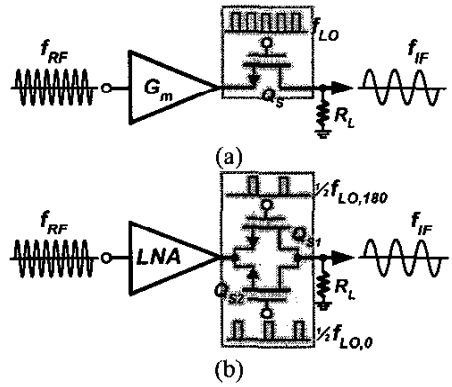
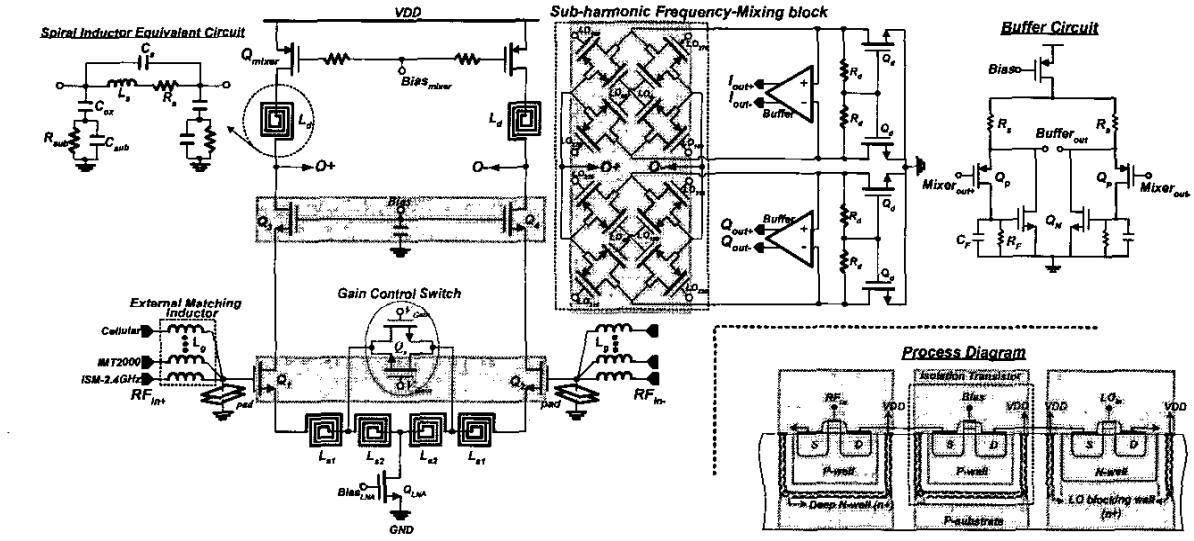


Fig. 1. (a) Conventional Mixer, (b) Sub-Harmonic Mixer

A. Low Noise Amplifier Design

The LNA is basically inductively degenerated cascode LNA, where resistive part of input matching is used for 50Ω matching. We use differential structure to eliminate common mode noise and to increase IIP2. Additional gain control circuits (transistor Q_s, inductor L_{s2}) are inserted to increase dynamic range. By switch-up V_{Gain} node to VDD or switch-down to GND, there are two gain modes, i.e. high gain mode and low gain mode respectively. The small signal equivalent circuit of the input part of the LNA is shown in Fig. 3, where g_m is trans-conductance of input transistor (Q_1), C_{gs}, C_{ps} mean the gate-source capacitance of Q_1 and parasitic capacitance of the switch transistor, Q_s. L_{lead}, L_{bond} and C_{pkg} are the lead-frame inductance, bond-wire inductance and package parasitic capacitance, respectively. Input



(a) (b)

Fig. 2. (a) Proposed merged structure of variable gain differential LNA and IQ SH-mixer, (b) LO to RF isolation by deep N-well

impedance (Z_{in1}), seen from the inside of the package of the IC, is expressed as

$$Z_{in1} = \frac{1}{SC_{gs}} + S\underbrace{\left(L_{s1} + \frac{L_{s2}}{1-w^2L_{s2}C_{gs}}\right)}_{\rightarrow L_{s1,2}} + \underbrace{\frac{g_m}{C_{gs}}\left(L_{s1} + \frac{L_{s2}}{1-w^2L_{s2}C_{gs}}\right)}_{\rightarrow R_{in}} \quad (3)$$

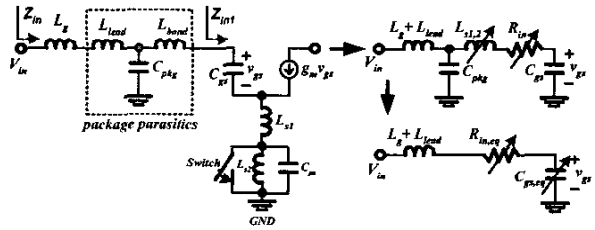


Fig. 3. Small signal equivalent circuit for half input part of the differential variable gain LNA

Resonance frequency of Z_{in1} is significantly changed during the switching operation. However, when considering the package parasitic components, the practical input impedance (Z_{in}) is expressed as following.

$$Z_{in} = SL_g + SL_{lead} + \frac{1}{SC_{pkg}} // (SL_{bond} + Z_{in1})$$

$$\cong \underbrace{\left(\frac{C_{gs}}{C_{pkg}+C_{gs}}R_{in}\right)}_{\rightarrow R_{in,eq}} + 1 \Big/ \underbrace{S\left(\frac{C_{gs}+C_{pkg}}{1-w^2L_{s1,2}C_{gs}}\right)}_{\rightarrow C_{gs,eq}} + S(L_g + L_{lead}) \quad (4)$$

In (4), bond-wire inductance is neglected, because we use double bonding to minimize bond-wire inductance in the input port. With typical value of 400fF for C_{pkg} in SSOP-28pin package and 100fF of C_{gs} for 100μm/1.8μm (W/L) of NMOS, the variation of $C_{gs,eq}$ is less than 10% at 2GHz, when $L_{s1,2}$ changes from 2nH to 8nH. So, gain control inductor L_{s2} doesn't significantly disturb overall matching characteristics during the switching operation. However, in case of noise consideration, C_{pkg} increases noise floor. NF for given LNA is expressed as (5), where $Q_{in} = w(L_g + L_{lead})/R_{in,eq}$ and γ is empirical constant.

$$NF = 1 + \gamma\frac{1}{R_{in,eq}}\left(\frac{C_{gs}+C_{pkg}}{C_{gs}}\right)\frac{1}{g_m}\frac{1}{Q_{in}^2} \quad (5)$$

To minimize NF, we use external high Q inductor for matching and the size of switch transistor is optimized to have small turn on resistance and not to lower Q_{in} by its parasitic capacitance.

B. Sub-Harmonic Mixer Design

As discussed previously, we use sub-harmonic mixer to eliminate DC offset problem. Specific sub-harmonic mixing principle can be explained from Fig. 4, where two parallel-connected transistors (Q_{s1}, Q_{s2}) act as frequency doublers. When biased near and less than threshold voltage, transistor Q_{s1} and Q_{s2} operate in saturation region alternatively in half period of the applied large LO signal.

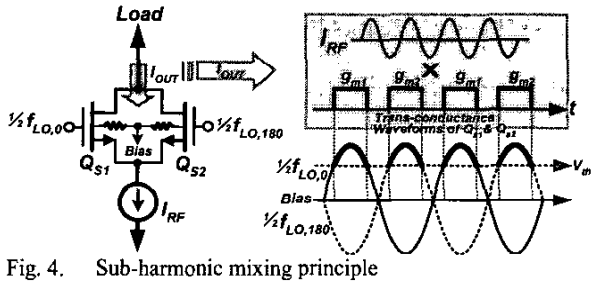


Fig. 4. Sub-harmonic mixing principle

Frequency of the overall trans-conductance of the parallel-connected transistor pairs is two times of the applied LO frequency as shown in Fig.4. By the mixing of this effective

trans-conductance and RF input signal, frequency down conversion is occurred. To reduce 1/f noise, we use PMOS transistor pairs as switching quad rather than NMOS and the transistors operate in sub-threshold region [3]. The mixer uses CMFB load to eliminate common mode DC offset. To increase isolation the PMOS switching pairs are located in an isolated N-well that is enclosed by P-substrate and deep N-well as shown in Fig.2 (b). Bias current of the mixer is supplied by Q_{mixer} which operate in triode region. To reduce loading effect at the mixer output, we use super source follower buffer [4].

C. *Interface between LNA and Mixer*

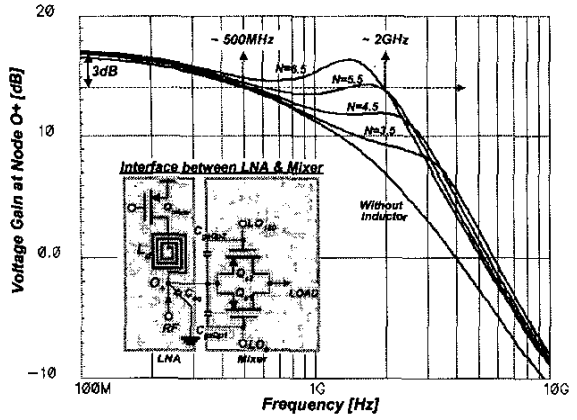


Fig. 5. Interface between LNA & mixer and bandwidth increment by inductive peaking at the interface

Table 1 Typical value of L_d

Turn Number (N)	3.5	4.5	5.5	6.5
Inductance [nH]	3.9	6.1	9.1	12.8
Q @2GHz	9.2	8.2	6.3	4.2

We merge LNA and mixer using inductively folded cascode structure to minimize noisy and non-linear elements, which is shown in Fig. 5, where resonance peaking phenomena according to different L_d are shown together. Typical value of L_d is shown in table 1. The impedance (Z_{O+}) of folding node (O_+) is expressed as $Z_{O+}= (SL_d+R_o)$ // $(1/SC_{tot})$ // $(1/G_{ms})$, where R_o is output impedance of Q_{mixer}, which supply bias current of LNA and mixer and operate in triode region. C_{tot} is overall parasitic capacitance of O_+ node and G_{ms} is effective overall trans-conductance of the switching transistors operating in sub-threshold region. Thus the peaking frequency (w_{peak}) is approximately expressed as following.

$$w_{peak} = \frac{1}{\sqrt{(1/Q^2+1)L_d C_{tot}}}, \quad Q = \frac{wL_d}{R_O} \tag{6}$$

Due to this resonance, 3dB-bandwidth can be increased to more than 2GHz by optimizing L_d and size of switching transistors. Overall size (W/L) of switching PMOS pairs is 480μm/1.8μm.

III. EXPERIMENTAL RESULTS AND DISCUSSION

The IC is fabricated using 0.18μm mixed-mode CMOS process (1P6M, triple-well) and housed in a SSOP-28pin plastic package. The fabricated chip photo is shown in Fig. 6 and overall size is 2.3mm×1.2mm. For measurement, we use 2-layer FR4 (ε_r=4.56) PCB and external balun transformer for single to differential signal conversion at the LNA input and I&Q LO input. Supply voltage is 1.8V and total bias current is 9.4mA.

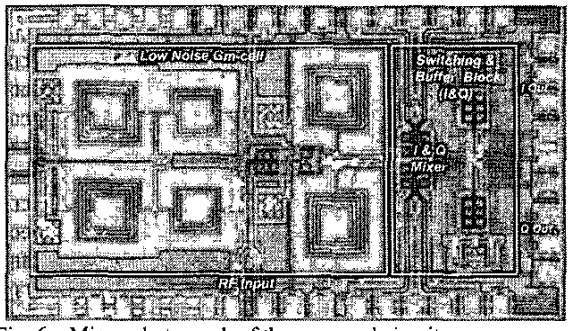


Fig. 6. Micro-photograph of the proposed circuits

Measurement results of S11 and noise characteristics at WCDMA band are shown in Fig.7, where measured noise PSD is divided by signal gain (25dB) and measurement loss (6dB) including cable and balun loss. Due to package parasitics (mainly C_{pkg} of 400fF), S11 has little changes during the change of gain modes. At high gain mode, DSB NF is 3.4dB and 4.7dB at IF of 2MHz and 200KHz respectively. Corner frequency of 1/f noise is approximately 100KHz.

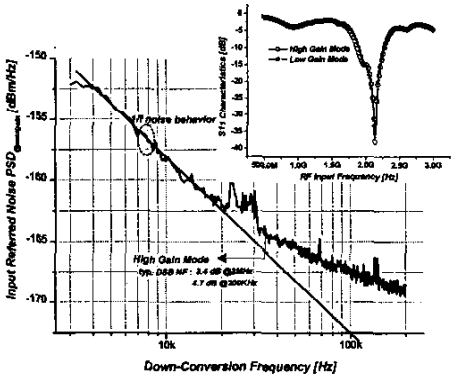


Fig. 7. S11 & noise characteristics at WCDMA band

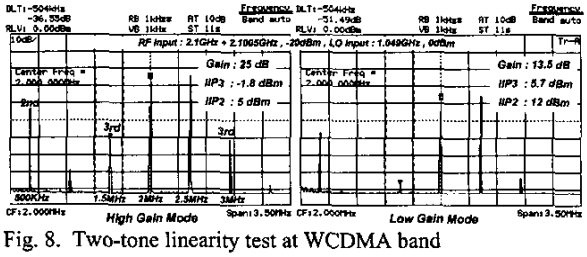


Fig. 8. Two-tone linearity test at WCDMA band

Two-tone linearity characteristics at WCDMA band are shown in Fig. 8. To compare DC offset suppression, we fabricated same structure of LNA and mixer of which the only difference is that the mixer uses conventional double balanced frequency mixing technique. The comparisons of DC offset and gain according to LO power are shown in Fig. 9, where offset suppression in case of sub-harmonic mixing is more than 30mV at 0dBm LO power.

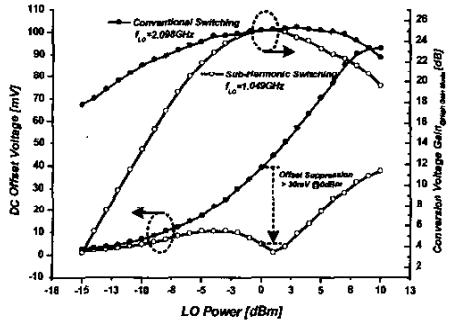


Fig. 9 Comparisons of DC offset voltage and gain characteristics according to LO input power (f_{RF}=2.1GHz, P_{RF}=-20dBm)

Table 2 Performance summaries at WCDMA band

	High Gain Mode	Low Gain Mode
RF frequency band	WCDMA (2110-2170 [MHz])	
LO frequency (center)	1072 [MHZ] (0dBm)	
Power Consumption	VDD=1.8V, IDD=9.4mA (LNA:6mA, IQ mixer:0.4mA, IQ buffer:3mA)	
SII [dB]	< -30 @2140[MHz]	
Gain [dB] @IF=2MHz	25	13.5
DSB NF [dB] @IF=2MHz	3.4	8.3
IIP2 [dBm]	5	12
IIP3 [dBm]	-1.8	5.7
Isolation(LO to RF) [dB]	< -50 @ f_{LO}=1.072GHz	
DC Offset [mV]	< 6 @ P_{RF}=-20dBm, P_{LO}=0dBm	
Technology	0.18mm CMOS (1P6M, triple-well)	

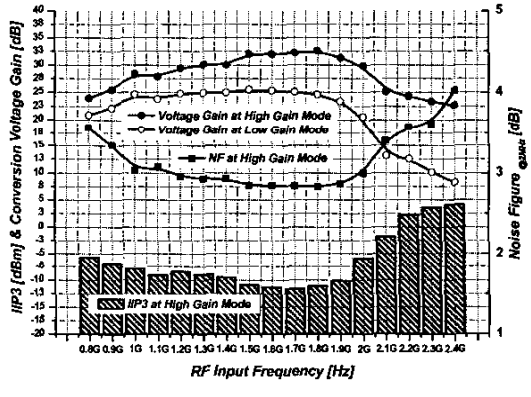


Fig. 10. Frequency responses of the voltage gain, NF and IIP3

Major measured figures at WCDMA band are summarized in Table 2. For multi-band application, measurement results of conversion gain, NF and IIP3 versus RF input frequency are shown in Fig. 10, where LO power and bias condition are same with the case of WCDMA band but L_g is chosen case by case for each frequency band. Typical value of L_g is 1.5nH and 35nH at 2.4GHz and 900MHz respectively. The major performance figures of high gain mode in various commercial wireless standards are summarized in Table 3.

Table 3 Performance summaries at wireless commercial bands

	S11 [dB]	Gain [dB]	NF [dB]	IIP3 [dBm]	IIP2 [dBm]
Cellular 900MHz	< -13	25.4	3.5	-7.1	12.6
GPS 1570MHz		32	2.9	-11	17.3
PCS 1850MHz		32	2.8	-10.5	7.7
IMT 2140MHz		25	3.4	-1.8	5
ISM 2400MHz		22.7	4.1	4.1	15

*. The above Gain, NF, IIP3 and IIP2 are measured at high gain mode of 2MHz down-conversion frequency.

IV. CONCLUSION

To implement multi-band direct conversion RF front-end, we design a new merged structure of differential variable gain LNA and mixer, which adopts inductively folded cascode structure to increase 3dB-bandwidth. The mixer use sub-harmonic mixing technique to reduce DC offset problem. To reduce 1/f noise, we use PMOS transistors as switching quads that operate in sub-threshold region. The IC is fabricated using 0.18μm 1-poly 6-metal CMOS technology and successfully works in the range from 800MHz to 2.4GHz with 17mW power consumption (V_{DD}=1.8V).

ACKNOWLEDGEMENT

This work is supported from the project of National Research Laboratory (NRL) that is sponsored by Korea Ministry of Science and Technology.

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